Application Note

Switched-Capacitor A/D Converter Input Structures

by
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CMOS has become popular as the technology for many modern A/D converters. CMOS offers good analog switches, good capacitors (although size is limited), and high digital logic density. These features have been combined to achieve a number of different A/D converter architectures. Many SAR-type (Successive Approximation Register) CMOS A/D converters utilize ratio-weighted capacitors, all controlled by analog switches and digital logic, to achieve conversion. Delta-sigma converters use analog switches and small capacitors for sampling. Conversion in a CMOS delta-sigma A/D converter is performed using a switched-capacitor comparator which samples at a much higher speed than the bandwidth of the signal to be converted. The comparator then presents a stream of ones and zeros to be processed to the digital filter portion of the chip. High CMOS logic density allows the digital filter to be orders of magnitude more complex than an analog filter while being drift-free and exactly repeatable from chip to chip.

The analog input of most CMOS A/D converters is constructed with analog switches and capacitors. Figures 1, 2, and 3 illustrate input structures commonly found in CMOS or BiCMOS A/D circuits. These three structures are common to capacitive-type SAR converters and to delta-sigma converters.

Figure 1 illustrates an unbuffered capacitive sampler. The size of the sampling capacitor and the frequency of the switch closure will deter-

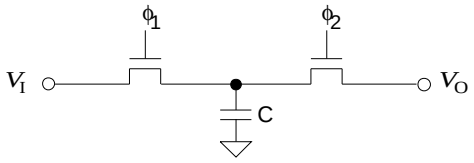

Figure 1. Unbuffered Capacitive Sampler

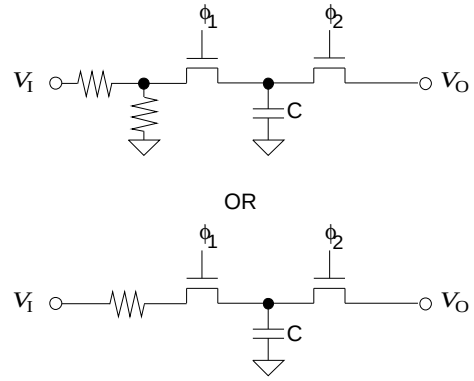

Figure 2. Unbuffered Capacitive Sampler with Resistor Input

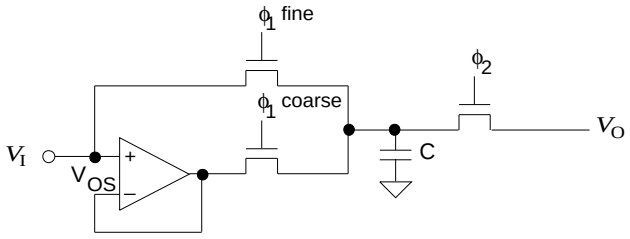

Figure 3. Coarse Charge Buffered Capacitive Sampler

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mine the severity of the dynamic load seen by the driving amplifier.

Figure 2 illustrates a capacitive sampler with an input resistor added. Input resistors are used in some A/D converters to divide down the input signal; for example, reducing ±10 volts down to ±2.5 volts. The signal reduction allows the circuitry internal to the converter to be powered from ±5 volts and still handle high level input signals. The resistors may introduce gain errors over temperature because of their limited tempco tracking. One bit at 16 bits is only about 15 ppm. The closest tempco tracking of the best resistor technologies is about 2 ppm/°C.

Some converters may use a single resistor at the input. The resistor reduces the transient current impulse seen by the external driving amplifier. The resistor also enables the external drive amplifier to see a resistive load instead of a more capacitive load. This improves the amplifier phase margin and reduces the possibility of ringing. The resistor enables the transient load current from the sampler to be spread over time due to the RC time constant of the circuit. A series resistance is usually acceptable in 12-bit designs, but it can hinder performance in fast 16-bit converters. The settling time of the RC network can limit the speed at which the converter can operate properly or reduce the settling accuracy of the sampler.

Figure 3 illustrates a coarse charge (also called rough charge) buffered capacitive sampler. The on-chip coarse charge buffer reduces the dynamic current demanded from the signal source because the coarse charge buffer precharges the sampling capacitor to a voltage nearly equal to the input signal.

The input structures in Figure 1 and 3 are most common. To understand the drive requirements of these two circuits, the input current required by the unbuffered sampler will be examined and its effective input resistance will be determined. Then it will be compared to the input current and effective input resistance of the coarse charge buffered sampler.

In Figure 1 the sampling capacitor, C is switched at a fixed frequency, f. The capacitor transfers a specific amount of charge each time the capacitor is switched. This charge is furnished by the signal source outside of the chip.

The size of the sampling capacitor and the frequency at which it is switched will determine the input current, and therefore, the effective input resistance of the sampler. Using the fundamental equations:

$$i = \frac{q}{t} \qquad q=cV$$

The instantaneous current is equivalent to the charge per unit time and charge is equivalent to the product of the capacitance and voltage, an equation which defines the input current to the unbuffered sampler (figure 1) can be developed:

$$i = C\frac{dV}{dt}$$

$$i = C(V_O - V_I)/\Delta t = C(V_O - V_I)f$$

Rearranging the equation, the effective input resistance can be shown to be:

$$\frac{V}{i} = R = 1/fC$$

From this equation it can be seen that the effective input resistance is inversely proportional to the sampling clock frequency. This indicates that if this sampler is part of an A/D converter which can operate over a wide range of clock frequencies, that as the device is operated at higher frequencies the input resistance goes down. This results in higher input current. Errors can be introduced because of the source impedance of the

external driving circuitry. Circuit behavior should be fully evaluated at whatever clock rate the circuit is going to be operated.

The coarse charge buffered sampler is shown in Figure 3. When the coarse switch is on (fine is off), the buffer coarse charges the capacitor to a voltage approximately equal to the input source voltage V_I. The advantage of the buffer is that the majority of the charging current needed to charge C is supplied by the coarse charge buffer and not by the signal source. This greatly reduces the current demand from the source outside the chip. The actual voltage output from the buffer will include whatever offset voltage exists in the buffer. When the coarse switch is off and the fine switch is on, the signal source will supply the current necessary to charge the sampling capacitor to its final value.

From the circuit the following equation can be derived for the input current:

$$i = V_{OS}/(1/fC) = fC\ V_{OS}$$

where 1/fC is the effective resistance of the switched capacitor circuit.

The equation indicates that the input current is independent of the input voltage and is a constant current which is a function of the sampling capacitor, the operating frequency, and the offset voltage of the buffer. Note that the polarity of the input current is affected by the polarity of the coarse charge buffer's offset voltage.

It is easy to see the advantage of a buffered sampler over an unbuffered sampler. In the buffered version of the sampling circuit, the signal source must furnish only enough charge to compensate for the offset of the buffer; whereas in the unbuffered sampling circuit (Figure 1), the signal source must furnish all of the charge necessary to charge the sampling capacitor.

This discussion has assumed that the sampling capacitor in each of the sampling circuits is fully discharged each time it is connected to the output circuit. Sometimes the output circuit is designed in such a way that it leaves the sampling capacitor charged at some particular voltage. This will affect the amount of charge that the unbuffered sampling circuit requires from the signal source.

The behavior of these sampling circuits will be affected if additional components are added between the outside driving amplifier and the input to the sampler. Two possible situations will be examined. First, the effect of adding a series resistance between the external drive amplifier and the A/D input will be investigated. Then the effect of adding a series resistor and a filter capacitor between the driving amplifier and the A/D input will be examined.

Effects of an External Resistor

Using the circuit illustrated in Figure 4, the behavior of the coarse charge buffered sampler will be examined with a resistor added between the output of the external signal source and the input

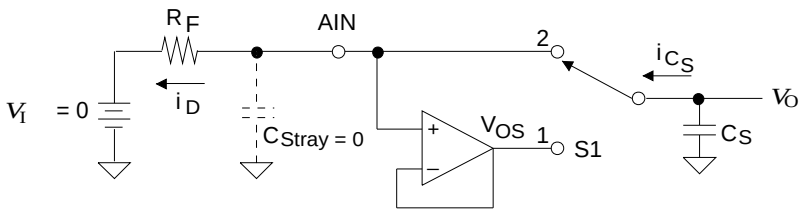

Figure 4. Buffered Sampler with External Source Resistance.

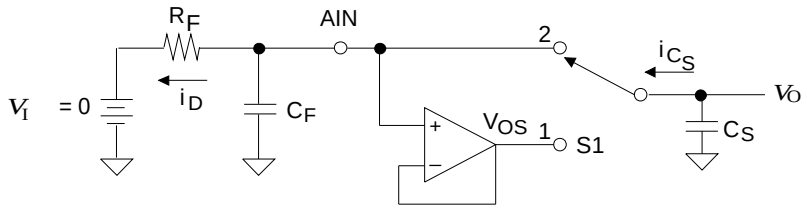

Figure 5. Buffered Sampler with External RC Filter.

to the sampler (Similar equations could be developed for the unbuffered sampler, but will not be done here). Assume that the input voltage $V_I = 0$ (the result will be the same for any constant input signal as the offset of the buffer is what dictates the charge requirement to settle the sampling capacitor to its final value). When the switch is in position 1, the sampling capacitor is charged to the voltage at the output of the internal buffer. Assume the offset of the buffer is such that the voltage on the sampling capacitor is a positive value, which will be called Vos. When switch S1 changes to position 2, the voltage on the sampling capacitor discharges to zero through the external source resistance (and the resistance of the switch if its value is significant relative to RF).

The internal sampling circuit will settle to full accuracy in the time that switch S1 is in position 2 if the external source resistance (R_F) is sufficiently low. The time available for settling is a function of the clock running the sampler. The sampler is usually connected to the input pin for one half clock cycle of the master clock. If the external resistance is too large, the sampling capacitor will be left with an error voltage when the sample time ends.

If the time that switch S1 is in position 2 is one half of a clock cycle, the voltage on C_S will discharge exponentially through source resistance R_F for t/2 where t is the period of one full clock cycle. The maximum source resistance for a given error voltage V_E is:

$$V_O = V_{OS}\, e^{-\frac{t}{2}/R_F C_S}$$

$$\ln\left(\frac{V_E}{V_{OS}}\right) = \frac{-t/2}{R_F C_S}$$

$$\ln\left(\frac{V_{OS}}{V_E}\right) = \frac{t/2}{R_F C_S}$$

$$R_{F_{max}} = \frac{1}{2f\, C_S \ln\left(\frac{V_{OS}}{V_E}\right)}$$

Effects of an External RC Filter

The case with an RC-filter placed at the input of the sampler will now be examined. Figure 5 illustrates this case.

The circuit will be analyzed with $V_I = 0$ (the result will be the same for any constant input signal as the offset of the buffer is what dictates the charge requirement to settle the sampling capacitor to its final value). When the switch is in position 1, the sampling capacitor is charged to the voltage at the output of the buffer. Assume the offset of the buffer is such that the voltage on the sampling capacitor is positive value called Vos. When at steady state

$V_{C_S} = V_{OS}$ S1 is in position 1.

$V_{C_S} = V_{C_F}$ S1 is in position 2.

The charge transfer rate from C_S to C_F during each clock cycle is

$$\Delta q = C_S(V_{OS} - V_{C_F})$$

Since $i = \frac{\Delta q}{\Delta t}$, $i_{C_S} = \frac{C_S (V_{OS} - V_{C_F})}{\Delta t}$ and $\frac{1}{\Delta t} = f$;
Therefore $i_{C_S} = f_{C_F}(V_{OS} - V_{C_F})$

In the steady state condition,

$$i_{C_S} = i_D$$

Therefore

$$V_{C_F}/R_F = fC_S(V_{OS} - V_{C_F})$$

where V_{C_F} is the error voltage V_E.

Therefore, for a given error voltage the maximum R_F should not exceed

$$R_F \leq \frac{V_E}{fC_S(V_{OS} - V_E)}$$

The equation applies only if

$$f >> \frac{1}{RC}$$

An external RC filter in front of the sampler lowers the bandwidth of the circuit and therefore reduces input noise. It also acts to isolate the transient current demand of the sampler from the external drive amplifier by allowing the sampler to draw its transient current out of the filter capacitor. This greatly reduces the transient current seen by the drive amplifier. Therefore, the amplifier is less likely to ring or overshoot due to the transient load. Adding an external RC filter can be detrimental if it has an excessively long time constant. This can cause the source resistance of the filter to introduce an offset error.

When an external amplifier drives either the unbuffered, or the buffered sampler directly, the amplifier may have difficulty with the transient load conditions. The transient load may cause the amplifier to exhibit ringing or oscillation. The behavior of the amplifier may vary as the signal amplitude changes; with the most common problems occurring with signals near zero crossover. A common symptom is for a user of a high speed A/D converter to suspect the converter of having a nonlinearity or of having missing codes in its transfer function; but the actual problem is that the driving amplifier is ringing and failing to settle at the proper signal level before the sample capacitor captures the signal. Some amplifiers will have more difficulty than others. An amplifier which exhibits peaking in its closed loop response will generally have more problems. To minimize the possibility of ringing, choose an amplifier which has gain rolloff which is linear for at least one decade of frequency above the frequency where the closed loop gain intersects with the open loop gain response. The amplifier circuit should be chosen or designed to achieve low output impedance at the sampling frequency of the capacitive sampler. A wideband amplifier with good drive current capability works best with a high speed A/D. The transient load seen by any amplifier can be reduced if an RC filter is added between the output of the operational amplifier and the input to the switched-capacitor sampler. The values for the resistor and capacitor are usually recommended by the A/D manufacturer. Making the time constant too large can reduce settling accuracy or produce an offset error in the circuit.

Other Circumstances Which Alter Input Behavior

Various A/D converter input structures have been discussed. It has been shown that the input seen by the external driver depends upon the size of the sampling capacitor, the sampling frequency, and whether or not the input is coarse charge buffered. The effect of an external source resis-

tance and the effect of an external RC filter have been discussed.

There are additional circumstances which can affect the input impedance. From the equation for the switched capacitor input impedance (R = 1/fC) it is readily understood that the dynamic load will change if the clock frequency to the sampler is changed. There are several conditions in which this can occur. The most common condition is that the master clock to the converter is modified. An example of this occurs in some applications of the CS5501/CS5503 converters. The CS5501/CS5503 converters include a low pass digital filter which has a -3 dB corner frequency of 10 Hz when operated with a master clock frequency of 4.096 MHz. If the clock frequency to the converter is lowered the corner frequency is reduced proportionately. Some measurement systems allow the user to select a slower converter clock to reduce the noise band width of the converter. This allows the converter bandwidth to be optimized for the noise conditions in the circuit. This change in clock rate will change the behavior of the input of the converter. This change in dynamic behavior can interact with the external driving circuitry and introduce errors in the measurement.

Input impedance can also change due to sampling clock changes which occur in converters that allow the user to modify the output word rate of the converter. Some first generation audio codecs would change the sample clock of the input stage whenever a different word rate was selected. Newer codecs keep the input stage sampling clock constant when the output word rate is changed.

Another example of the converter's input impedance being affected, can occur in instrumentation converters which include a PGA (Programmable Gain Amplifier) stage as part of the input stage of the converter. These converters allow the gain to be modified by changing the size of the sampling capacitor, or by modifying the sample rate of the capacitor sampler. Either of these will alter the converter's input impedance if the gain change is performed at the input stage of the converter. The CS5516 and CS5520 include a PGA, but it is placed after an input instrumentation amplifier. The instrumentation amplifier input impedance remains constant when the PGA gain is changed. Products from other vendors modify the input stage to accomplish gain changes and therefore alter the input impedance of the converter.

This application note has discussed the drive requirements of CMOS A/D converters. While the discussion has been applied to the input for the signal to be converted, realize that this discussion can apply to the voltage reference input pins of the converter as well.